REMARKS

Claims 2, 4, 5, 8, 9, 11, 13 and 14 are pending in this application. By this Amendment, claims 2 and 11 and the title are amended and claims 1, 3, 6, 7, 10 and 12 are cancelled. Reconsideration and allowance of the above-identified Application in view of the above amendments and the following remarks are respectfully requested.

The title was objected to as not being clearly indicative of the invention. In response, applicant has amended to title to recite a "Method of Manufacturing a Semiconductor Device Without Oxidized Copper Layer." Applicant respectfully submits that the amended title is more descriptive. Reconsideration and withdrawal of the objection are respectfully requested.

Claims 4, 8 and 13 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 6, 218,303 to Lin. This rejection is respectfully traversed.

Lin discloses the formation of a via using oxide reduction of an underlying copper. Lin discloses an integrated circuit having a substrate 10, a local-interconnect structure 12, and a metal-interconnect structure 14. The silicon substrate 10 is doped to define active circuit regions such as source 20, drain 22, and channel 24. The local interconnect structure 12 includes a tungsten source contact 30, a tungsten drain contact 32, a polysilicon gate 34, a gate oxide 36, and a silicon dioxide submetal dielectric 38. The metal interconnect structure 14 includes a first metal layer 40, an intermetal dielectric layer 42, a second metal layer 44, and a passivation layer 46. The first metal layer 40 defines first metal layer conductors 50 and contact vias 52. The first metal layer 40 is formed by a damascene process. (See column 3, lines 29-31). No reduction step is used to prepare for deposition of the first metal layer 40. (See column 4, lines 43-44). The first metal layer 40 includes a first tantalum barrier sublayer 54 and a first copper bulk-conductor sublayer 56. A second metal layer 44 defines second metal layer conductors 60 and intermetal vias 62. Second metal layer comprises a second tantalum barrier sublayer 64 and a second copper bulk-conductor sublayer 66. The second metal layer is also formed by a damascene process.

By contrast, claim 4 is directed to a method of manufacturing a semiconductor device. The method includes forming a first insulating layer on a semiconductor substrate. A first conductive line is formed by depositing a conductive material on the first insulating layer and selectively patterning the conductive material. A second insulating layer is formed by

depositing an insulating material on top of the substrate including on the first conductive line. A via hole if formed by selectively patterning the second insulating layer in order to expose a certain portion of the first conductive line. A natural oxide layer, which formed on the first conductive line through natural oxidation of the first conductive line, is then removed by heat treating in an H_2+CO gas atmosphere.

Lin does not disclose the method disclosed in claim 4. In particular, Lin does not disclose to claimed formation of the first conductive line. As set forth in claim 4, the first conductive line is formed by depositing a conductive material on the first insulating layer and selectively patterning the conductive material. Instead, Lin uses a damascene process to form the first metal layer 40. Lin does not selectively pattern a conductive material deposited on the first insulating layer. Accordingly, Lin does not disclose, teach or suggest the subject matter of claim 4.

By contrast, claim 8 is directed to a method of manufacturing a semiconductor device. The methods includes forming a first insulating layer on a semiconductor substrate. A first conductive line is formed by depositing a conductive material on the first insulating layer and selectively patterning the conductive material. A second insulating layer is formed by depositing an insulating material on top of the substrate including on the first conductive line. A via hole and a trench are formed by selectively patterning the second insulating layer to expose a certain portion of the first conductive line. A metal barrier is then formed by depositing a metal layer on top of the substrate including in the via hole and on the trench. A copper seed layer is formed on top of the metal barrier. A natural copper oxide layer, which formed on the copper seed layer through natural oxidation of the copper oxide layer, is removed by heat treating in an H_2+CO gas atmosphere.

Lin does not disclose the method disclosed in claim 8. In particular, Lin does not disclose to claimed formation of the first conductive line. As set forth in claim 8, the first conductive line is formed by depositing a conductive material on the first insulating layer and selectively patterning the conductive material. As discussed above, Lin uses a damascene process to form the first metal layer 40. Lin does not selectively pattern a conductive material deposited on the first insulating layer. Furthermore, Lin discloses removing the oxidation formed on the first metal layer before sputtering a copper seed layer. Lin does not disclose removing the copper oxide layer on the copper seed layer. Accordingly, Lin does not disclose, teach or suggest the subject matter of claim 8.

By contrast, claim 13 is directed to a method of manufacturing a semiconductor device. The methods includes forming a first insulating layer on a semiconductor substrate. A first conductive line is formed by depositing a conductive material on the first insulating layer and selectively patterning the conductive material. A second insulating layer is formed by depositing an insulating material on top of the substrate including on the first conductive line. A via hole and a trench are formed by selectively patterning the second insulating layer to expose a certain portion of the first conductive line. A metal barrier if formed by depositing a metal layer on top of the substrate including in the via hole and on the trench. A conductive material is deposited for forming a conductive line on top of the substrate including on the metal barrier to sufficiently fill the via hole and the trench. A plug and a second conductive line are then formed by planarizing the conductive material on the second insulating layer in order to expose the second insulating layer. A natural oxide layer, which formed on the second conductive line through natural oxidation of the second conductive line, is then removed by heat treating in an H_2+CO gas atmosphere.

Lin does not disclose the method disclosed in claim 13. In particular, Lin does not disclose to claimed formation of the first conductive line. As set forth in claim 13, the first conductive line is formed by depositing a conductive material on the first insulating layer and selectively patterning the conductive material. As discussed above, Lin uses a damascene process to form the first metal layer 40. Lin does not selectively pattern a conductive material deposited on the first insulating layer. Furthermore, Lin discloses removing the oxidation formed on the first metal layer before sputtering a copper seed layer. Lin does not disclose removing the copper oxide layer on the copper seed layer. Accordingly, Lin does not disclose, teach or suggest the subject matter of claim 13.

Applicant respectfully submits that claims 4, 8 and 13 define subject matter patentable over Lin. Reconsideration and withdrawal of the rejection based upon Lin is respectfully requested.

Claims 1-3, 5-7, 9-12 and 14 were rejected under 35 U.S.C. § 103(a) over Lin, as applied to claims 4, 8 and 13, in view of U.S. Patent No. 6, 090,701 to Hasunuma et al. This rejection is respectfully traversed.

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In response, claims 1, 3, 6, 7, 10 and 12 are cancelled. As such, the grounds for the rejection are now moot. Applicant reserves the right to pursue a continuation application directed to the subject matter in these claims.

The Office Action relies on Hasunuma for allegedly teaching removing the natural oxide layer using heat treatments. Hasunuma, however, does not disclose, teach or suggest any of the deficiencies in Lin discussed above in connection with claims 4, 8 and 13. Accordingly, the combination of Lin and Hasunuma do not disclose, teach or suggest the subject matter of these claims. Claims 2 and 5 depend from claim 4. Claim 9 depends from claim 8. Claims 11 and 14 depend from claim 13. These claims are allowable over Lin and Hasunuma for at least the reasons set forth above. Reconsideration and withdrawal of the rejection based upon Lin and Hasunuma are respectfully requested.

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Respectfully submitted,
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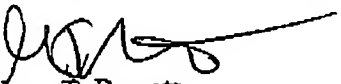

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